AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the

application:

LISTING OF CLAIMS:

1. (original): A gallium nitride compound semiconductor multilayer structure comprising

a substrate, and an n-type layer, a light-emitting layer, and a p-type layer formed on the substrate,

the light-emitting layer having a multiple quantum well structure in which a well layer and a

barrier layer are alternately stacked repeatedly, said light-emitting layer being sandwiched by the

n-type layer and the p-type layer, wherein the well layer comprises a thick portion and a thin

portion, and the barrier layer contains a dopant.

2. (original): A gallium nitride compound semiconductor multilayer structure according

to claim 1, wherein the well layer contains In.

3. (original): A gallium nitride compound semiconductor multilayer structure according

to claim 2, wherein the upper surface of the well layer is covered with a thin layer not containing

In.

4. (currently amended): A gallium nitride compound semiconductor multilayer structure

according to claim 1 any one of claims 1 to 3, wherein the dopant is at least one member selected

from the group consisting of C, Si, Ge, Sn, Pb, O, S, Se, Te, Po, Be, Mg, Ca, Sr, Ba, and Ra.

2

Appln. No.: National Stage of PCT/JP2005/003428

5. (currently amended): A gallium nitride compound semiconductor multilayer structure according to claim 1 any one of claims 1 to 4, wherein the dopant is contained at a concentration of 1×10^{17} cm⁻³ to 1×10^{19} cm⁻³.

6. (currently amended): A gallium nitride compound semiconductor multilayer structure according to claim 1 any one of claims 1 to 5, wherein the thick portion has a thickness of 1.5 nm to 5 nm.

7. (currently amended): A gallium nitride compound semiconductor multilayer structure according to <u>claim 1 any one of claims 1 to 6</u>, wherein the thick portion has an arithmetic mean width, as measured in a cross-section of the multilayer structure, of 10 nm or more.

8. (currently amended): A gallium nitride compound semiconductor multilayer structure according to claim 1 any one of claims 1 to 7, wherein the thin portion has a thickness of less than 1.5 nm.

9. (currently amended): A gallium nitride compound semiconductor multilayer structure according to <u>claim 1</u>-any one of claims 1 to 8, wherein the thin portion has an arithmetic mean width, as measured in a cross-section of the multilayer structure, of 100 nm or less.

Appln. No.: National Stage of PCT/JP2005/003428

10. (currently amended): A gallium nitride compound semiconductor multilayer structure according to claim 1 any one of claims 1 to 9, wherein the difference in thickness between the

thick portion and the thin portion falls within a range of 1 nm to 3 nm.

11. (currently amended): A gallium nitride compound semiconductor multilayer structure

according to claim 1 any one of claims 1 to 10, wherein the thick portion has a total width, as

measured in a cross-section of the multilayer structure, accounting for 30% or more the entire

width of the well layer.

12. (currently amended): A gallium nitride compound semiconductor multilayer structure

according to claim 1 any one of claims 1 to 11, wherein the multiple quantum well structure is

repeatedly stacked 3 to 10 times.

13. (currently amended): A gallium nitride compound semiconductor multilayer structure

according to claim 1 any one of claims 1 to 12, wherein the barrier layer is formed of a gallium

nitride compound semiconductor selected from among GaN, AlGaN, and InGaN which has an In

content lower than that of InGaN forming the well layer.

14. (original): A gallium nitride compound semiconductor multilayer structure according

to claim 13, wherein the barrier layer is formed of GaN.

4

Appln. No.: National Stage of PCT/JP2005/003428

15. (currently amended): A gallium nitride compound semiconductor multilayer structure according to <u>claim 1</u> any one of claims 1 to 14, wherein the barrier layer has a thickness of 7 nm to 50 nm.

16. (original): A gallium nitride compound semiconductor multilayer structure according to claim 15, wherein the barrier layer has a thickness of 14 nm or more.

17. (currently amended): A gallium nitride compound semiconductor light-emitting device, wherein the device has a negative electrode and a positive electrode, the negative electrode and the positive electrode being provided on the n-type layer and the p-type layer of a gallium nitride compound semiconductor multilayer structure according to claim lany one of elaims 1 to 16, respectively.

18. (original): A gallium nitride compound semiconductor light-emitting device according to claim 17, which has a flip-chip-type device structure.

19. (original): A gallium nitride compound semiconductor light-emitting device according to claim 18, wherein the positive electrode has a reflection-type structure.

Appln. No.: National Stage of PCT/JP2005/003428

20. (currently amended): A gallium nitride compound semiconductor light-emitting device according to claim 17 any one of claims 17 to 19, wherein an operation voltage falls within a range of 2.9 V to 3.2 V at a current of 20 mA.

- 21. (currently amended): A gallium nitride compound semiconductor light-emitting device according to <u>claim 17</u> any one of claims 17 to 19, wherein a take-off voltage falls within a range of 2.5 V to 3.2 V.
- 22. (currently amended): A lamp comprising a gallium nitride compound semiconductor light-emitting device according to claim 17any one of claims 17 to 21.
- 23. (currently amended): A lamp comprising a fluorescent material and a gallium nitride compound semiconductor light-emitting device according to <u>claim 17.any one of claims 17 to</u>
 21.
- 24. (original): A method for producing a gallium nitride compound semiconductor multilayer structure comprising a substrate, and an n-type layer, a light-emitting layer, and a p-type layer formed on the substrate, the light-emitting layer having a multiple quantum well structure in which a well layer and a barrier layer are alternately stacked repeatedly, said light-emitting layer being sandwiched by the n-type layer and the p-type layer, wherein the method

Appln. No.: National Stage of PCT/JP2005/003428

comprises forming a thick portion and a thin portion in the well layer by doping the barrier layer with a dopant.

- 25. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 24, wherein the dopant is contained at a concentration of 1×10^{17} cm⁻³ to 1×10^{19} cm⁻³.
- 26. (currently amended): A method for producing a gallium nitride compound semiconductor multilayer structure according to <u>claim 1 any one of claims 1 to 16</u>, wherein the method comprises a step of forming the well layer, which step includes a step of growing a gallium nitride compound semiconductor and a step of decomposing or sublimating a portion of the gallium nitride compound semiconductor.
- 27. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 26, wherein the step of growing is performed at a substrate temperature of T1 and the step of decomposing or sublimating is performed at a substrate temperature of T2, wherein T1 and T2 satisfy the relationship: T1≤T2.
- 28. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 27, wherein T1 falls within a range of 650 to 900°C.

Appln. No.: National Stage of PCT/JP2005/003428

29. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 28, wherein T2 falls within a range of 700 to 1,000°C.

30. (currently amended): A method for producing a gallium nitride compound semiconductor multilayer structure according to <u>claim 27any one of claims 27 to 29</u>, wherein the step of decomposing or sublimating is performed while the substrate temperature T1 is elevated to T2.

- 31. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 30, wherein the substrate temperature T1 is elevated to T2 at a temperature elevation rate of 1°C/min to 100°C/min.
- 32. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 31 above, wherein the temperature elevation rate is 5°C/min to 50°C/min.
- 33. (currently amended): A method for producing a gallium nitride compound semiconductor multilayer structure according to <u>claim 30any one of claims 30 to 32</u>, wherein the substrate temperature T1 is elevated to T2 over 30 seconds to 10 minutes.

Appln. No.: National Stage of PCT/JP2005/003428

34. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claims 33, wherein the substrate temperature T1 is elevated to T2 over one minute to five minutes.

- 35. (currently amended): A method for producing a gallium nitride compound semiconductor multilayer structure according to <u>claim 27</u> any one of claims 27 to 34, wherein the barrier layer is grown at T2.
- 36. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 35, wherein the barrier is grown at T2, followed by lowering the substrate temperature to T3 at which further growth is performed.
- 37. (original): A method for producing a gallium nitride compound semiconductor multilayer structure according to claim 36, wherein T3 is equal to T1.
- 38. (currently amended): A method for producing a gallium nitride compound semiconductor multilayer structure according to <u>claim 26any one of claims 26 to 37</u>, wherein the step of growing is performed in an atmosphere containing a nitrogen source and a Group III metal source and the step of decomposing or sublimating is performed in an atmosphere containing a nitrogen source but no Group III metal source.